Array of serially connected silicon CMOS sub-terahertz detectors per pixel architecture

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Summary

Integrated silicon detector pixel is presented in 90 nm CMOS technology with 52 kV/W@0.47 THz response. In a pixel, four antenna coupled detector FETs are connected in series to improve SNR. The response is amplified, digitalized and filtered by integrated lock-in amplifier. Motivations are discussed of multiple detectors per pixel.

Introduction

Several integrated antenna coupled field effect transistor based sub-THz detector have been published. From imaging point of view, the current solutions use whiskbroom setup up to a dozen of integrated pixels [1,2,5]. This presentation highlight consequences of imagers of low numeric aperture (NA) optics and/or solid immersion lens (SILs) in conjunction with the resonant antenna size, gives reasons why to implement an array of small detectors within a single pixel.

Focal plane spot size

The imaging optics found in sub-THz imaging literature varies from simple reflective elements – parabolic mirrors – to refractive solutions, including SILs. Reflective optics are applied - possibly combined at the detector by hemispherical lens - more widely due to its advantages when the spectral band of interest spread over broad region. The stand-off imaging favours e.g. Cassegrian telescopes [1], while transmission imaging typically based on off-axis parabolic mirrors in whiskbroom setups [2]. In the focal plane, the diffraction limited spot size is $\lambda_0(2\times NA)$, note that in open space coupling typical reported values of NA are 0.05-0.2, with HR silicon SILs the effective NA~1 [5, 6].

Antenna coupled detector size

The radiation must be collected and focused to the detector. The basic element of RF microelectronic technologies, the integrated planar antenna serves this purpose. Let us focus on those cases, when the antenna cannot be shielded from the substrate (typically broadband designs). In general, the effective permittivity of the high permittivity substrates, like silicon or GaAs, tunes the fundamental resonant length ($L_r$) of an antenna well below under its free space counterpart ($L_0$) [3]. E.g. the resonant length of a dipole implemented on silicon substrate becomes this way appr. 2.5 times smaller ($\lambda_r = \lambda_0(\varepsilon_{\text{eff}})^{1/2}$, $\varepsilon_{\text{eff}} = (\varepsilon_{\text{si}} + 1)/2$, $L = \lambda/2$, where $\varepsilon_{\text{si}} = 11.7$ and $L_0$: $L_r \sim 1:0.4$). In immersion optics the shortening of resonant length stronger, for Si reaches $L_0$: $L_r \sim 1:0.3$.

Based on the above considerations, the resonant antenna area at a certain wavelength coupled to a detector is smaller than the reasonable spot size in both
systems (at silicon substrate, with f/3.2 optics this area ratio would be 1:15). Note that this ratio does not depend on the wavelength, only on the optics and the substrate.

**Array of small units of serially connected detectors**

The proposed solution is an array of optimally resonating antenna detectors connected in series to cover the spot size. The reason against one larger antenna are the followings: i) both systems capture the same energy having near identical effective size, but the larger one has lower peak frequency, collecting less energy at the desired frequency; ii) though serially connected FET detectors worsen the noise performance, but the sensitivity and noise increases linearly and proportional to the square root of the number of detectors [4], respectively. Hence the SNR improves choosing the array too.

The presented pixel architecture is the part of a 4x3 array implemented in 90 nm CMOS technology. It comprises four serially connected 120° flare angle bow-tie antenna coupled detectors in series (Fig 2), a low-noise amplifier, and a voltage controlled oscillator for digitalizing the signal (Fig 1.). Post-processing is performed by the on-chip digital lock-in amplifier. The pixel provides 52 kV/W@0.47 THz amplified sensitivity, which is 3.1 times larger than its double sized single antenna version.

![Diagram of pixel architecture](image1)

**Fig 1. Architecture of the pixel.**

![Microphoto of a pixel](image2)

**Fig 2. Microphoto of a pixel.**

**References**